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Do 254 For Fpga Designer

DO-254 for the FPGA Designer - Xilinx

DO-254 for the FPGA Designer By: Dagan White 2 wwwxilinxcom WP401 (v101) March 7, 2012 DO-254 - The General DO-254 - The General DO-254, Design Assurance Guidance for Airborne Electronic Hardware [Ref 1], provides guidance for design assurance in airborne electronic hardware (AEH) to ensure safe operation Rather than specify how to implement the standard or which test should be

Xilinx WP403 Practical Use of FPGAs and IP in DO-254 ...

certification staff can use and apply DO-254 when working on certification projects This order also provides guidance to the designer, yet gray areas still exist regarding the application of DO-254 in FPGA development Although DO-254 addresses design assurance of hardware up to and including the line replaceable unit (LRU), the FAA

DO-254: Challenges and Solutions

level, the DAL has implications in terms of what needs to be followed for the DO-254 process The FPGA or ASIC designer works with a designated engineering representative (DER) of the FAA (in the US) to achieve compliance to the appropriate standard level The final stage of demonstrating compliance involves testing the hardware item in the end system (usually at the board level) Once this

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RTCA/DO-254 COMMERCIAL-OFF-THE-SHELF GRAPHICAL ...

Programmable Gate Arrays (FPGA) and Application Specific Integrated Circuits (ASIC) can use DO-254 to comply with airworthiness regulations Section 112 of RTCA/DO-254 addresses the use of commercial off the shelf (COTS) components in safety critical aircraft systems COTS components are commercially available devices such as a graphics

A Procedure to Verify and Validate an FPGA Level Testing ...

A Procedure to Verify and Validate an FPGA Level Testing as Per DO-254 Dr Manju Nanda#, P Rajshekhar Rao* #,*Aerospace Electronics & Systems Division, CSIR- National Aerospace Laboratories, Bangalore, Karnataka, India Abstract:-This paper describes the how advanced verification

Application of DO-254 Level A (Appendix B) Design ...

As part of DO-254's guidance, Level A & B programs are to implement Advanced Verification according to Appendix B Of the suggested methodologies Elemental Analysis is most often implemented by conducting a coverage analysis of a PLD/FPGA/ASIC design at the VHDL (design coding language) level of abstraction What this is really accomplishing

Military Productivity Factors in Large FPGA Designs

Figure 2 Integration Becomes More Significant as FPGA-Based Design Sizes Grow DO-254 and Other Certifications Defense designs have special requirements beyond those of the normal commercial designs and tool chains The one currently affecting defense designs the most is Design Assurance Guidance DO-254 for aviation safety Others

Effective Verification for DO-254 Projects

— “Achieving Quality and Traceability in FPGA/ASIC Flows for DO-254 Aviation Projects” — “The Use of Advanced Verification Methods to Address DO-254 Design Assurance” — “Effective Functional Verification Methodologies for DO-254 Level A/B and Other Safety-Critical Devices”

Advanced Verification Techniques for DO-254

Advanced Verification Techniques for DO-254 Test and Verification Solutions Mike Bartley (mike@testandverification.com) Delivering Tailored Solutions for

Enabling Model-Based Design for DO-254 Compliance with ...

1 White paper Enabling Model-Based Design for DO-254 Compliance with MathWorks and Mentor Graphics Tools www.mathworks.com The purpose of RTCA/DO-254 ...

FPGA Familiarization - (Introduction to Field Programmable ...

software development This session introduces Field Programmable Gate Array (FPGA) technology and development This is intended for engineers and management who need to understand FPGAs, but who do not intend to personally develop FPGA designs The attendee will leave with a solid foundation of FPGA technology, development process, and

DO-254 Training - YongaTek

- FPGA Level In-Target Testing o DO-254/CTS Day4 - Objectives: • ALDEC DO-254 Flow will be explained Instructor- Roy Vandermolen Electronic designer with over 35 years of experience in electronics Currently a Staff Engineer and Certification Manager for electronic flight control systems at Moog Aircraft and an airborne electronics hardware Outside Boeing Authorized Representative (...

Qualification of Tools for Airborne Electronic Hardware

88 Radiation Effects and FPGA Architectures 50 89 Radiation—DO-254 and DO-160 51 810 What Circuit Is Being Generated 51 811 Unused Inputs and Outputs 52 812 Other Considerations 52 813 Power Up/Reset Issues 53 814 What Can Be Done to Prevent Problems 53 815 Design Issues

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Automated traceability to assist DO-254 certification

Automated traceability to assist DO-254 certification Andy Nicol, Principal Firmware Engineer 2 - d Agenda • Company Overview • Firmware Engineering group overview • DO-254 and the problem of traceability • What is ReqTracer and how does it help? • Example outputs • Example use case • Pros and cons of ReqTracer • Summary • Questions 3 - d Finmeccanica Airborne

ALDEC Safety-Critical Solutions DO-254

• RTCA/DO-254 • FPGA Flow for DO-254 Compliance • Aldec DO-254 Solutions • DO-254 Training and Consulting Services • Requirements Management and Traceability • HDL Coding Standards • FPGA Design and Simulation • Code Coverage • FPGA Level In-Target Testing o DO-254/CTS Day1 - ...

Vol. 5, Issue 5, May 2016 DO-254 Implementation of CAN for ...

achieve DO-254 compliance Design requirements are tracked by ReqTracer along with the test results throughout the entire product development cycle, ultimately providing real-time measurement of progress Code is created in the HDL Designer such that the pre-defined DO-254 coding rules are met This helps in ...

FPGA Design Solution for High-Reliability Applications

FPGA Design Solution for High-Reliability Applications ``Design Automation for High Reliability ``FPGA Technology Independence ``Best Quality of Results for High Performance ``Integrated SEU Mitigation Technologies ``Supports Industry Standards for DO-254, IEC 61508, and ISO 26262 ``Signal Processing IP and Verification ``Industry Leading RTL Synthesis Technology

Simplified UVM for FPGA Reliability UVM for “Sufficient ...

Simplified UVM for FPGA Reliability UVM for “Sufficient Elemental Analysis” in DO-254 Flows by Shashi Bhutada, Mentor Graphics 51 DERs would like a tool that showed the spec in an executable format for stimulus and response This can reduce the time currently spent on manual audit Managers would like to eliminate unnecessary redundant waste of simulation cycles and designer’s time

Best FPGA Development Practices - jps-pcb.com

Best FPGA Development Practices In Advisory Circular 20-152, the edeFral viationA Administration AA)(F recommends DO-254 TCA/DO-R 254 Design Assurance Guidance orF Airborne Electronic Hardware de nes simple electronics and states that if it is not simple, it is complex